## CLAIMS

1. A method for decoding variable length codes, said method comprising:

receiving a stream comprising a first plurality of variable length codes and a second plurality of variable length codes;

decoding the first plurality of variable length codes;

storing one or more symbols from the second plurality of variable length codes in a first register;

storing a portion of a particular symbol from the second plurality of variable length codes in the first register;

storing another portion of the particular symbol in a second register; and

storing the contents of the first register in memory after storing the portion of the particular symbol from the second plurality of variable length codes in the first register.

2. The method of claim 1, further comprising:

storing one or more symbols from the second plurality of variable length codes in the second register;

storing a portion of another particular symbol from the second plurality of variable length codes in the second register;

storing another portion of the another particular symbol in the first register; and

storing the contents of the second register in memory after storing the portion of the another particular symbol from the second plurality of variable length codes in the second register.

3. The method of claim 2, the contents of the first register and the contents of the second register being stored in adjacent locations in the memory.

4. The method of claim 1, the register and the memory being characterized by a width, the width of the register and the width of the memory being equal.

5. A system for decoding variable length codes, said system comprising:

a presentation buffer for receiving a stream comprising a first plurality of variable length codes and a second plurality of variable length codes;

a processor for decoding the first plurality of variable length codes;

a first register for storing one or more symbols from the second plurality of variable length codes and a portion of a particular symbol from the second plurality of variable length codes;

a second register for storing another portion of the particular symbol; and

memory for storing the contents of the first register after storing the portion of the particular symbol from the second plurality of variable length codes in the first register.

6. The system of claim 5, the second register storing one or more symbols from the second plurality of variable length codes, and a portion of another particular symbol from the second plurality of variable length codes;

the first register storing another portion of the another particular symbol; and

the memory storing the contents of the second register after storing the portion of the another particular symbol

from the second plurality of variable length codes in the second register.

7. The system of claim 6, the contents of the first register and the contents of the second register being stored in adjacent locations in the memory.

8. The system of claim 5, the register and the memory being characterized by a width, the width of the register and the width of the memory being equal.

9. A circuit for decoding variable length codes, said circuit comprising:

a processor connected to the data memory; and

memory storing a plurality of instructions executable by the processor, the plurality of instructions comprising:

decoding the first plurality of variable length codes;

writing one or more symbols from the second plurality of variable length codes in a first register;

writing a portion of a particular symbol from the second plurality of variable length codes in the first register;

writing another portion of the particular symbol in a second register; and

writing the contents of the first register in memory after storing the portion of the particular symbol from the second plurality of variable length codes in the first register.

10. The system of claim 9, wherein the plurality of instructions further comprise:

storing one or more symbols from the second plurality of variable length codes in the second register;

storing a portion of another particular symbol from the second plurality of variable length codes in the second register;

storing another portion of the another particular symbol in the first register; and

storing the contents of the second register in memory after storing the portion of the another particular symbol from the second plurality of variable length codes in the second register.

11. The system of claim 10, the contents of the first register and the contents of the second register being stored in adjacent locations in the memory.

12. The system of claim 9, the register and the memory being characterized by a width, the width of the register and the width of the memory being equal.